ISSN: 2277-9655
Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

DESIGN AND MODELLING HILBERT TRANSFORM BASED PHASE DETECTOR FOR ALL DIGITAL PHASE LOCKED LOOP

Anupama Patil*, Dr P.H.Tandel
Electronics and Communication Dept Pacific Academy for Higher Education and Research Udaipur

DOI: 10.5281/zenodo.51007

ABSTRACT

The Phase Locked Loop (PLL) is an almost always used electronics circuit for communication systems like modulator, demodulator, frequency generator and frequency synthesizer etc. All-digital phase locked loop (ADPLL) is digital version of the PLL. In this paper, a novel Hilbert transform based phase detection system for all-digital phase locked loop (ADPLL) is presented. The digital discrete time components are used to realize the phase detector system reducing the complexity of the design. The Hilbert transform based phase detection system provides a definite advantage over conventional analog phase detectors with both sinusoidal and its Quadrature signal. The studied system is modelled and tested in the MATLAB/Simulink environment.

KEYWORD: ADPLL, PLL, Hilbert transform, Phase detector.

INTRODUCTION

With the growth of the wireless communication system, the demand of the stable circuits at high frequency has increased dramatically. The band 2GHz to 4GHz (S band), 4GHz to 8GHz (C band) 8GHz to 12.5GHz (X band) are presently in use for the communication. Hence the compatible electronics is required to use for the generation and detection of wireless signal. To fulfil this requirement, use of the digital component in wireless communication is preferable. Phase-Locked Loop (PLL) is an electronic feedback circuit which is most common circuit for wireless communication system. PLL circuit locks a feedback signal phase relative to input reference signal. It is use to realize the modulator, and demodulator, frequency generator and frequency synthesizer etc. The block diagram of continuous PLL is shown below,

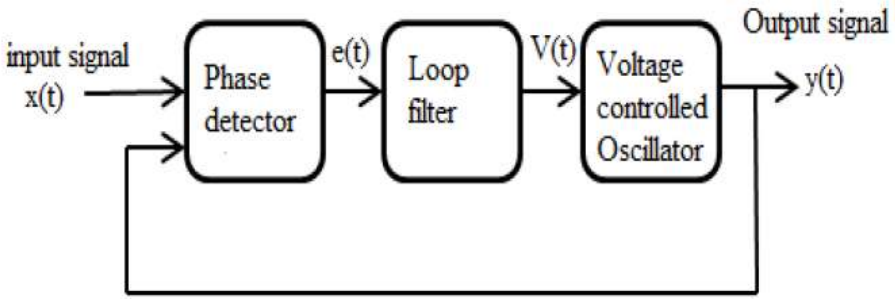

Figure 2: Block diagram of PLL

PLL are classified into various categories as shown in Table 1 [1].

Table 1 Comparison of various types of phase locked loops

PLL	Phase detector or comparator	Loop filter	Voltage or digital controlled oscillator
Analog or linear Phase Locked Loop	Analog	Analog	Analog
Digital Phase Locked Loop	Digital	Analog	Analog
All Digital Phase Locked Loop	Digital	Digital	Digital

ISSN: 2277-9655
Impact Factor: 3.785

This paper focussed on the All-Digital Phase Locked Loop which is a highly demanding component in wireless communication due to its robustness. This is a type of PLL in which all the components are in digital sending and receiving signals in digital form. It can hence be very well realized using FPGA.

Survey on All-digital phase locked loop (ADPLL)

Many researchers have been working in the field of ADPLL. The improved FPGA implementation is the key point of the work. However, researcher also has explored the algorithm improvement. Martin Kumm has presented their work on implementation of ADPLL using FPGA in 2010 [2]. A generic design of digital discrete-time All-digital phase locked loop (ADPLL) using Hilbert transforms and CORDIC method has been realized. This design uses only 15% of FPGA resources. The provides an analytical solution for locking frequency range and stability range. Digital phase locked loop [3] was designed for clock generation in the range of GHz. The bandwidth tracking technique was used to provide stable operation across frequency range without calibration. Chia-Tsun et al. [4] have designed a fast-lock engine to improve lock-in time using Frequency Estimation Algorithm. A 2.4-GHz low power ADPLL was given by Liangge Xu [5]. This All-digital phase locked loop (ADPLL) design is suitable for Industrial, scientific and medical band applications in wireless systems such as wireless local area network (WLAN), Bluetooth and Zigbee where low-power is required. This design, delay based technique is used to reduce TDC power dissipation. Deok-Soo Kim et al. [6] have proposed Adaptive loop gain controller (ALGC) to reduce the non-linearity of bang-bang phase frequency detector and output jitter. In 2011, YoungGun Pu et al. [7] have introduced low power All-digital phase locked loop (ADPLL) having wide range and high resolution Time to Digital converter. In this design, phase interpolator and time amplifier improves the resolution of Time to Digital converter. By using fine resolution of Digital Controlled Oscillator, the phase noise is improved. Xin Chen et al. [8] have designed fast locking All-digital phase locked loop (ADPLL) using feed-forward compensation technique. In this implemented design of All-digital phase locked loop (ADPLL) has two modes: frequency acquisition mode and phase acquisition mode. The fast frequency locking in frequency acquisition mode and linear phase locking in phase acquisition mode is achieved by ADPLL. A digital phase locked loop [9] with Time to Digital converter (TDC) is implemented using a new concept of floating point number representation which is scaled in resolution according to the amount of input difference. The weinjing Yin et al. [10] have proposed bandwidth and tuning range technique to reduce jitter and power consumption. Chao-Ching Hung et al. [11] have proposed Bang-Bang Algorithm for fast locking. Davide Tasca et al. [12] have proposed a ÄÓ fractional-N Digital Phase Locked Loop based on single bit Time to Digital converter (TDC). In this design, the quantization noise can be cancelled out by placing TDC (digital to time converter) in feedback path and benefits like low noise, low power are achieved.

Digital phase detection using Hilbert transform:

The concept of analytic signal is used in order to obtain the phase information of the signal. The analytic signal as the property that it has no negative frequency components. Any real sinusoid signal can be converted to a positive frequency complex sinusoid by simply generating a phase quadrature component to serve as the imaginary part. For complicated signals consisting of sum of many sinusoids, a filter is used which shifts each component by a quarter cycle. These types of filters are called Hilbert Transform Filters.[13]

The analytic signal is generated by applying Hilbert transform to the real signal and using it as the imaginary part to extend the original signal. Let a signal $v1(t)$ is given as

$$v1(t) = \cos(\omega_0 t + \theta_e) \quad (1)$$

Then,

$$\theta_e = \tan^{-1}\left[\frac{\cos\omega_o t \cos(\omega_o t+\theta_e) + \sin\omega_o t \sin(\omega_o t+\theta_e)}{\cos\omega_o t \sin(\omega_o t+\theta_e) + \sin\omega_o t \cos(\omega_o t+\theta_e)}\right] \quad (2)$$

One form of implementation of Hilbert transformer phase detector is as shown in the block diagram of figure 1.

ISSN: 2277-9655
Impact Factor: 3.785

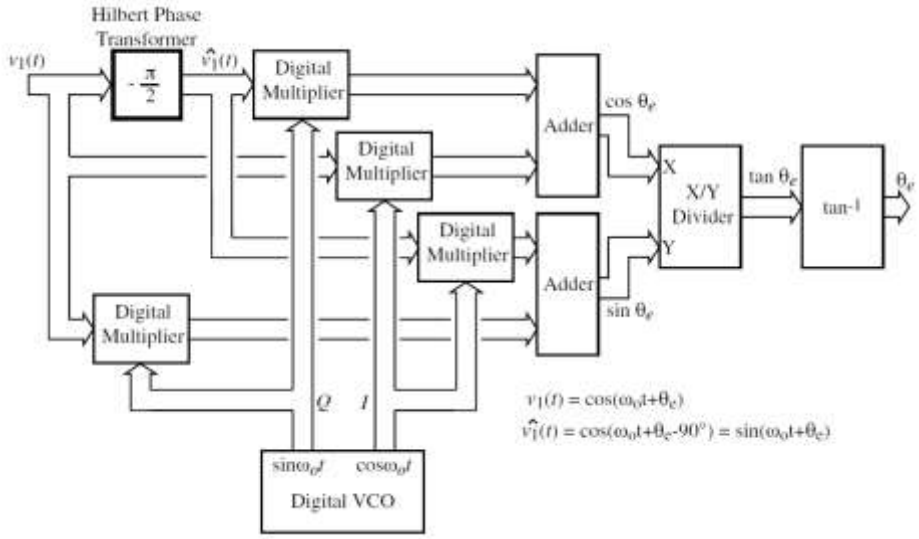

Figure 3: Block diagram of phase detector using Hilbert transform [14]

MATLAB simulation

Two discrete sine wave sources have been used for finding the response of the phase detector. The Simulink diagram of the test bench is shown below.

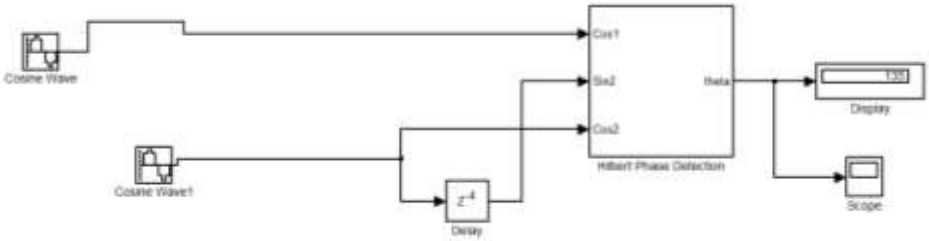

Figure 4: Simulink Model of phase detector using Hilbert transform

Hilbert phase detection model:

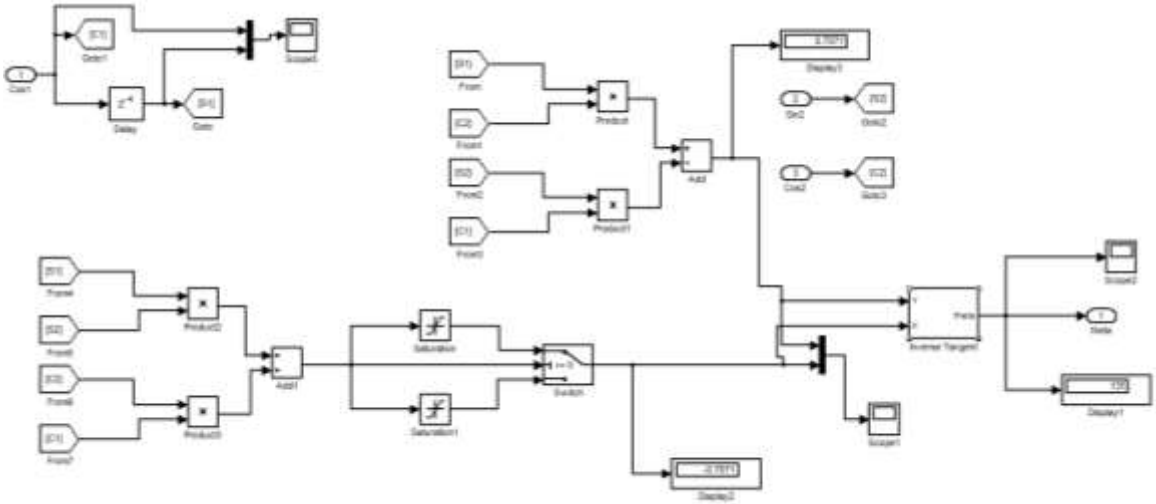

Figure 5: Detail of Simulink model of phase detector

ISSN: 2277-9655
Impact Factor: 3.785

RESULTS

The following parameters have been used for the detection of the signal.

Table :2 Input parameters

S. No.	Parameter	Value
1	Frequency of signal	249 MHz and 250 MHz
2	Sampling Time	0.25 ns
3	Signal amplitude	1

The model has been simulated for different phases. The detected output for different condition is given below ,Phase track for phase difference 5*pi/4 (225°).

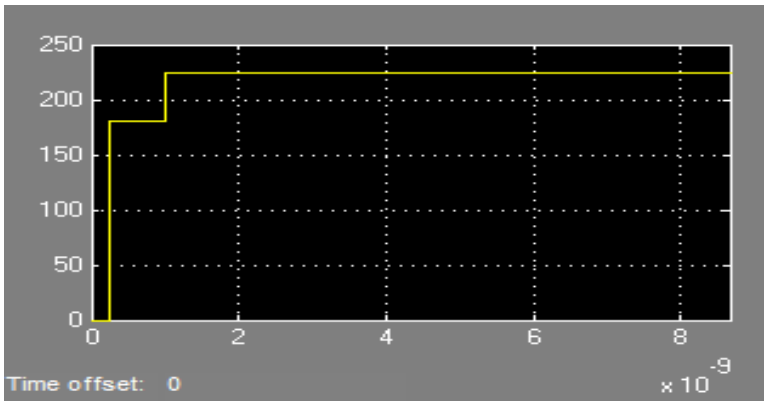

Figure 6: Phase detector output with time
Phase track for phase difference 3*pi/4((135°).

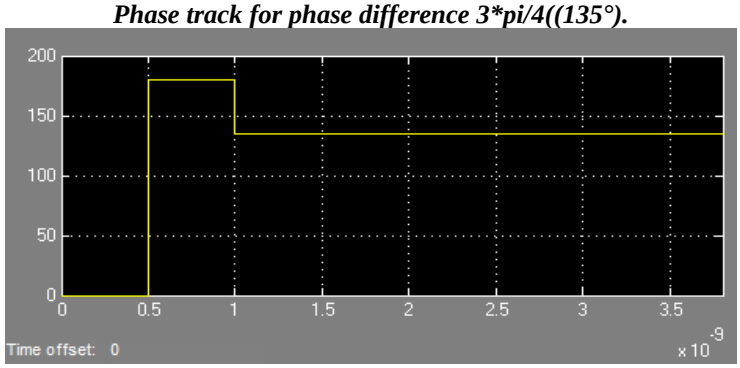

Figure 7: Phase detector output with time for phase difference 135°
Phase track for frequency difference of 1 MHz

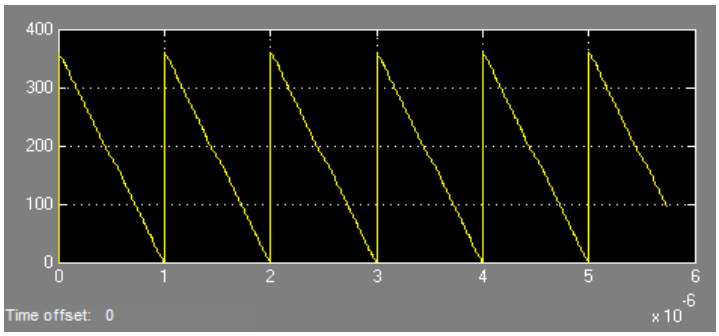

Figure 8: Phase detector output with time for frequency difference of 1 MHz

CONCLUSION

The phase detector model has been developed successfully. The maximum three sample clock is required to track the phase. The Simulink results generate the confidence to develop the FPGA block of the phase detector for ADPLL.

REFERENCE

[1] Varsha Prasad and Dr Chirag Sharma, "A Review of Phase Locked Loop", International Journal of Emerging Technology and Advanced Engineering, vol 2, no.6, pp.98-104, June 2012.
[2] Martin Kumm, HaraldKlingbeil and Peter Zipf, "An FPGA-Based Linear All-Digital Phase-Locked Loop", IEEE Transactions on Circuits and Systems,vol.57, no. 9, pp.2487-2497, Sept 2010.
[3] Ping-Hsuan Hsieh, Jay Maxey and Chih-Kong Ken Yang, "A Phase-Selecting Digital Phase-Locked Loop With Bandwidth Tracking in 65 nm CMOS Technology", IEEE Journal of Solid-State Circuits, vol. 45, no.4, pp.781-792, April 2010.
[4] Chia-Tsun Wu, Wen-Chung Shen, Wei Wang and An-Yen Wu, "A Two-Cycle Lock-In Time ADPLL Design Based on a Frequency Estimation Algorithm", IEEE Transaction on Circuits and Systems-II, vol.57, no.6, pp.430-434, June 2010.
[5] Liangge Xu, Saska Lindfors, Kari Stadius and Jussi Ryynanen, "A 2.4-GHz Low-Power All-Digital Phase-Locked Loop", IEEE Journal of Solid-State Circuits, vol.45, no.8, pp.1513-1521, Aug 2010.
[6] Deok-Soo Kim, Heesoo Song, Taeho Kim, Suhwan Kim and Deog-Kyoon Jeong, "A 0.3-1.4 GHz All-Digital Fractional-N PLL with Adaptive Loop Gain Controller", IEEE Journal of Solid-State Circuits, Vol.45, no.11, pp.2300-2311, Nov 2010.
[7] YoungGunPu, AnSoo Park, Joon-Sung Park and Kang-Yoon Lee, "Low-Power, All Digital Phase-Locked loop with a Wide-Range, High Resolution TDC", ETRI Journal, vol. 33, no.3, pp.366-373, June, 2011.
[8] Xin Chen, Jun Yang and Long-Xing Shi, "A Fast Locking All-Digital Phase-Locked Loop via Feed-Forward Compensation Technique", IEEE Transactions on Very Large Scale Integration(VLSI) Systems, vol.19, no.5, pp.857-868, May 2011.
[9] Young-Hun Seo, Seon-Kyoo Lee and Jae-Yoon Sim, "A 1-GHz Digital PLL With a 3-ps Resolution Floating-Point-Number TDC in a 0.18μm CMOS', IEEE Transactions on Circuits and Systems-II, vol.58, no.2, pp.70-74, Feb 2011.
[10] Wenjing Yin, "A 0.7-to-3.5 GHz 0.6-to-2.8mW Highly Digital Phase-Locked loop With Bandwidth Tracking", IEEE Journal of Solid-State Circuits, vol. 46, no. 8,pp.1870-1880, Aug 2011.
[11] Chao-Ching Hung and Shen-Iuan Liu, "A 40-GHz Fast-Locked All-Digital Phase-Locked Loop Using a Modified Bang-Bang Algorithm", IEEE Transactions on Circuits and Systems-II, vol.58, no.6, pp.321-325, June 2011.
[12] Davide Tasca, Marco Zanuso, Giovanni Marzin, Salvatore Levantino, Carlo Samori and Andrea L. Lacaita, "A 2.9-4.0-GHz Fractional-N Digital PLLWith Bang-Bang Phase Detector and 560-fsrms Integrated Jitter at 4.5-mW Power", IEEE Journal of Solid-State Circuits, vol.46, no.12, pp.2745-2758, Dec 2011.
[13] Abhishek Das, Suraj Dash, B.Chitti Babu and Ajit Kumar Sahoo, "A Novel Phase Detection System for Linear All-Digital Phase Locked Loop". IEEE 2012.
[14] http://users.ece.gatech.edu/pallen/Academic/ECE_6440/Summer_2003/L080-ADPLL(2UP).pdf